A Table-Based Bias and Temperature-Dependent Small-Signal and Noise Equivalent Circuit Model

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***Abstract*— A new algorithm is presented for construction of accurate table-based bias and temperature dependent field-effect transistor (FET) small-signal and noise models. The algorithm performs two-dimensional (2-D) linear interpolation on a single stored data table to quickly produce bias and temperature-dependent model simulations. Comparisons of simulated FET S-parameters, noise figure, and device figures of merit (e.g., $G_{\max}$) versus measured data show the model to be accurate over a wide range of bias and temperatures. Model enabled simulations of a single-stage FET-based low-noise monolithic microwave integrated circuit (MMIC) amplifier are also shown to compare favorably with measured amplifier data. The new algorithm improves on previously available approaches in three ways: 1) it allows efficient and accurate small signal device and circuit simulations over bias and temperature; 2) it allows circuit optimization with respect to bias and temperature; and 3) it provides substantial data storage reduction over alternate approaches. Because one compact data table represents a single sample device, the approach can be readily adapted for use in a statistical FET model data base.**

I. Introduction

MICROWAVE circuits using field effect transistors (e.g., MESFET's and HEMT's), or FET's, are subjected to thermally induced RF/microwave performance changes due to internal power dissipation and/or changes in the ambient temperature. Intentional or unintentional changes in the bias voltages across the gate-to-source (VGS) and drain-to-source (VDS) terminals also cause changes in FET performance. In fact, proper adjustment of bias conditions in symphony with temperature changes can compensate for temperature effects on RF/microwave performance [1]. For efficient and thorough circuit design, a means is needed to simulate the bias and temperature dependent behavior of FET based circuits. For receiver circuitry, efficient simulation of bias dependent small signal and noise performance is of interest, along with prediction of temperature induced performance changes.

One "brute force" approach to simulating the effects of changes in bias and thermal conditions is to directly utilize multiple sets of stored S-parameter and noise parameter data. Data are needed at each and every bias and temperature condition of interest, and data storage requirements are considerable with this approach. As an example, a typical S-parameter data file consists of four complex numbers stored at 201 frequency points for a total of 1608 stored numbers. A typical noise parameter data file consists of four noise parameters stored at 16 frequencies, or 64 stored numbers. Now assume that we want to characterize the device at ten values of VDS and ten values of VGS and at five temperatures for each bias condition. The total number of S-parameter and noise parameter data sets would be 500, requiring a total of 836 000 [i.e., $500 \times (1608 + 64)$] stored numbers. As can be seen, not only is the storage requirements for the 500 data sets large, but it is also very cumbersome to manage such a large number of files.

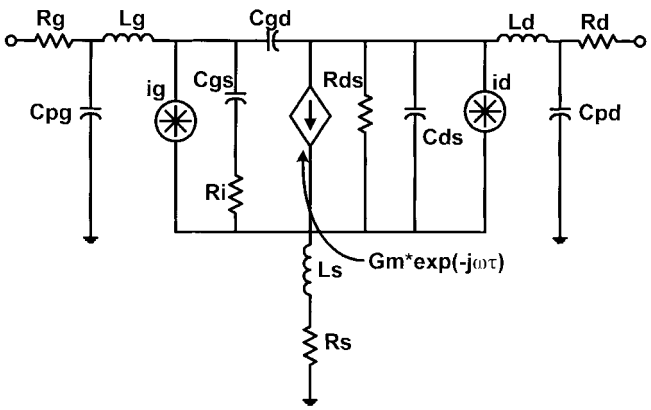

Fig. 1. Schematic of the small-signal and noise model.

A refinement on this approach would be to extract small-signal and noise models of the FET at the biases and temperatures of interest and then insert these models one at a time into the design simulation. Fig. 1 shows the schematic of a small signal and noise model FET model used in this work. The model is very similar to models found in the literature and requires 19 parameters. For the example discussed above, data storage requirements for this "conventional equivalent circuit model" approach would be 500×19 stored numbers or 9500. Thus, the equivalent circuit approach alone provides an order of magnitude reduction in the data storage requirement. However, this approach is inefficient because the engineer must manually input a different equivalent circuit model into the simulator for simulation at each bias and temperature condition.

Another solution to the problem would be to use a temperature-dependent nonlinear model [2]. This approach is the most efficient in terms of data storage requirements since the model would require about 100 parameters or less to describe the MESFET over bias and temperature. Unfortunately, temperature-dependent nonlinear modeling

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requires an extensive modeling effort and may prove inadequate due to failure of the empirical model equations to represent the device under small-signal conditions [3]. Also bias and temperature-dependent noise models are typically not integrated into available nonlinear models, though some work has been reported on bias-dependent noise models [4].

Recently, a novel table-based small-signal and noise field-effect transistor (FET) modeling approach was introduced [5]. The new modeling approach utilizes a single compact two-dimensional (2-D) table containing temperature model coefficients of equivalent circuit and noise model parameters. This provides further data reduction over the conventional equivalent circuit model approach. A simple algorithm used in conjunction with this table comprises a flexible and powerful bias and temperature-dependent small-signal and noise model. Two-dimensional linear interpolation of the data table produces accurate model simulations even at operating conditions not measured. The new modeling algorithm improves on previously available approaches in three ways: 1) it allows automated analysis; 2) it allows circuit optimization with respect to bias and (if desired) temperature; and 3) it provides for substantial data reduction over either the "brute force" data storage approach or the conventional equivalent circuit model approach. The current paper expands on this idea and presents additional results that include a model-enabled comparison, over bias and temperature, results for a single-stage MMIC low-noise amplifier. In addition to the application results presented in the current paper, a variation of this modeling approach has also been applied to modeling the bias-dependent behavior of cascode-connected FET pairs [6].

II. Modeling Methodology

A. Procedure for Bias and Temperature MESFET and HEMT Modeling

The small-signal and noise model used in this work is shown in Fig. 1. It is assumed that the extrinsic equivalent circuit parameters or (ECP's) (i.e., $R_s, R_d, R_g, L_s, L_d, L_g, C_{pg}$, and C_{pd}) are considered to be dependent on temperature but independent of bias. The intrinsic ECP's (i.e., $G_m, G_{ds}, C_{gs}, C_{gd}, C_{ds}, R_i, \tau$) are considered to be both temperature and bias dependent. It should be noted that only ambient temperature changes are considered here. Self-heating due to applied bias (small in low-noise devices) is not addressed. The noise current sources i_g and i_d in Fig. 1 model the noise of the intrinsic FET. We consider the noise sources to be correlated and the normalized noise correlation matrix is given by

$$\begin{bmatrix} |i_g i_g^*| & |i_g i_d^*| \\ |i_g^* i_d| & |i_d i_d^*| \end{bmatrix} = \begin{bmatrix} \dfrac{\omega^2 C_{gs}^2 R}{g_m} & \omega C_{gs}\sqrt{RP}C \\ \omega C_{gs}\sqrt{RP}C^* & g_m P \end{bmatrix} \quad (1)$$

where P, R, and C are noise model parameters that characterize i_g and i_d [7]. The noise model parameters P, R, and C are also considered to be both temperature and bias dependent.

The small-signal and noise model is extracted from measured S-parameter and noise parameter measurements. First, we extract the ECP's over bias and temperature. The ECP's were extracted using direct extraction methods [8]. The extrinsic ECP's were extracted from measured "cold-FET" and "pinched-FET" S-parameters at different temperatures. It is assumed that at each temperature the extrinsic ECP's are not bias dependent. The intrinsic ECP's were extracted from measured "hot-FET" S-parameters over a 2-D grid of bias points and over temperature. The results of the above extraction procedures are temperature-dependent extrinsic ECP's and bias and temperature-dependent intrinsic ECP's.

Next, we extract the noise model parameters P, R, and C over bias and temperature. Since the noise sources only model the noise of the intrinsic FET, the noise contribution of the parasitic resistances must be de-embedded from the total measured noise of the device. To de-embed the noise contribution of the parasitic resistances, we used a method described by Ikalainen [9] to arrive at the noise characteristics of the intrinsic FET. Using Ikalainen's method, the normalized intrinsic noise correlation matrix was generated over frequency using HP-EEsof's Libra 5.0 NMAT simulation. The noise of the intrinsic device was then modeled by the equation

$$\begin{bmatrix} \dfrac{\omega^2 C_{gs}^2 R}{g_m} & \omega C_{gs}\sqrt{RP}C \\ \omega C_{gs}\sqrt{RP}C & g_m P \end{bmatrix} = \begin{bmatrix} \mathrm{Re}(\mathrm{NMAT}[1,1]) & \mathrm{NMAT}[1,2] \\ \mathrm{NMAT}[2,1] & \mathrm{Re}(\mathrm{NMAT}[2,2]) \end{bmatrix}. \quad (2)$$

For this work P, R, and C values determined at 12 GHz were sufficient to use over the 2–18-GHz frequency range. The noise model parameters are frequency independent. Experimentally, the frequency dependence of the noise model parameters may exhibit an upward dispersion at low microwave frequencies due to the influence of gate leakage currents upon the measured noise parameters [10], [11]. These dispersions can be deembeded from the intrinsic FET by removing an equivalent conductance at the gate-to-source and gate-to-drain terminals [12]. The above procedure was repeated at each bias and temperature point resulting in P, R, and C values that are functions on bias and temperature.

The intrinsic ECP's and noise model parameters determined above form surfaces that are functions of three independent variables: VGS, VDS, and T. The task at hand is a three-dimensional (3-D) interpolation problem. Although 2-D interpolation schemes do exist and are given in the literature, 3-D interpolation schemes are rarely discussed. However, it is possible to break this 3-D interpolation problem into a one-dimensional (1-D) and a 2-D interpolation problem.

We first model the temperature dependence of the intrinsic ECP's and noise model parameters by a linear function of temperature. Over the considered temperature range of 25 °C–125 °C, each ECP and noise coefficient versus temperature can be modeled by a linear function [13], [14]. In this paper the following simple linear equation is used:

$$f_i(T) = m_i \cdot T + b_i \quad (3)$$

where $f_i(T)$ represents a particular ECP or noise model parameters over temperature and m_i and b_i are the corresponding

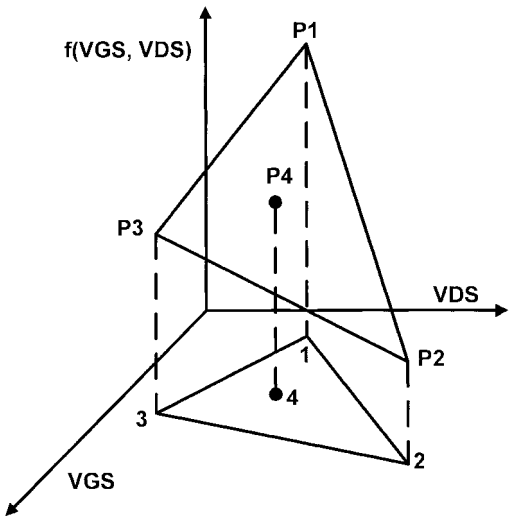

Fig. 2. Linear interpolation on a triangular facet.

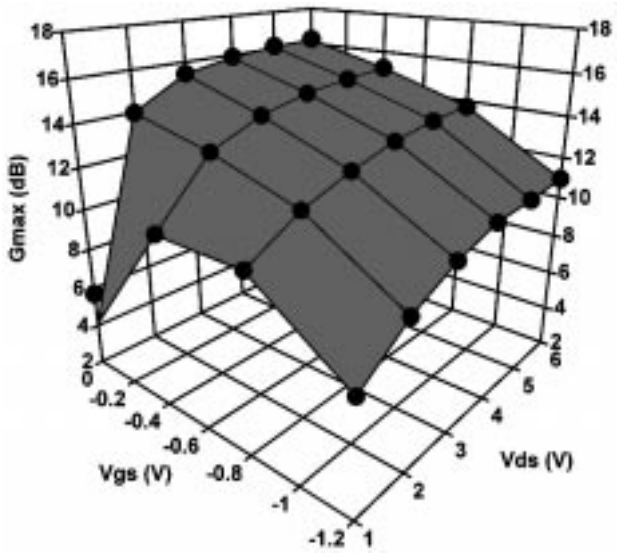

Fig. 3. Comparison of simulated versus measured $G_{\max}$ over gate and drain bias. The mesh lines represent the simulated data surface, and the dots represent measured data points. The data presented in the plots is for the 0.25 μm × 300 μm MESFET at $T = 25\,^{\circ}\mathrm{C}$ and $f = 14$ GHz.

temperature model coefficients or TMC's. The TMC's can be determined analytically by solving the over determined least square problem if there are more than two temperatures involved. TMC's for each ECP and noise model parameter are determined over bias resulting in a set of bias-dependent TMC's. The bias-dependent TMC's determined above are tabulated and stored in a model data file. Our model is programmed to read in a model data file and perform linear interpolation on the tabulated model values.

At this stage, the 3-D interpolation problem is now reduced to a 2-D interpolation problem: that of interpolating the TMC's over bias. Piecewise 2-D linear interpolation is used to calculate the TMC's for each ECP and noise model parameters at the desired bias.

B. A Method for 2-D Linear Interpolation

Given a set of n numbered points $P_n(\mathrm{VGS}_n, \mathrm{VDS}_n)$, the surface formed by the points can be approximated as a series of connecting triangular facets. In Fig. 2, for a triangular facet with vertices $P_1(VGS_1, VDS_1), P_2(VGS_1, VDS_1)$, and $P_3(VGS_1, VDS_1)$, the plane intersecting the three points is given by

$$P(\mathrm{VGS}, \mathrm{VDS}) = -\frac{a}{c}(\mathrm{VGS} - VGS_1) - \frac{b}{c}(\mathrm{VDS} - VDS_1) + P_1 \quad (4)$$

where

$$a = (VDS_2 - VDS_1)(P_3 - P_1) - (VDS_3 - VDS_1)(P_2 - P_1) \quad (5)$$

$$b = (P_2 - P_1)(VGS_3 - VGS_1) - (P_3 - P_1)(VGS_2 - VGS_1) \quad (6)$$

and

$$c = (VGS_2 - VGS_1)(VDS_3 - VDS_1) - (VGS_3 - VGS_1)(VDS_2 - VDS_1). \quad (7)$$

Hence the entire surface can be approximated by a piecewise application of (4).

Before interpolation on the a particular facet can be performed, the facet containing the point to be interpolated must be located. If P_4 (see Fig. 2) is the point to be interpolated, in the VGS–VDS plane, a search is made to find four points that form the smallest quadrilateral containing the point (VGS_4, VDS_4). This procedure is valid only for rectangular bias grids. If it is necessary, the procedure can be generalized to apply to nonrectangular grids. Once the quadrilateral is found, it is subdivided into two triangles. The next step is to determine which triangle contains the point (VGS_4, VDS_4).

The determination of whether a point is inside or outside a triangle is a classic problem in the area of computer science [15]. First, the three vertices of the triangle are numbered clockwise 1, 2, and 3 with the desired point being 4 (see Fig. 2). Next the following quantities are calculated:

$$a = \begin{vmatrix} V_{gs1} & V_{ds1} & 1 \\ V_{gs2} & V_{ds2} & 1 \\ V_{gs3} & V_{ds3} & 1 \end{vmatrix}, \quad b = \begin{vmatrix} V_{gs4} & V_{ds4} & 1 \\ V_{gs1} & V_{ds1} & 1 \\ V_{gs2} & V_{ds2} & 1 \end{vmatrix}$$

$$c = \begin{vmatrix} V_{gs4} & V_{ds4} & 1 \\ V_{gs2} & V_{ds2} & 1 \\ V_{gs3} & V_{ds3} & 1 \end{vmatrix}, \quad d = \begin{vmatrix} V_{gs4} & V_{ds4} & 1 \\ V_{gs3} & V_{ds3} & 1 \\ V_{gs1} & V_{ds1} & 1 \end{vmatrix}. \quad (8)$$

In (8) we are only concerned with the sign of a, b, c, and d and not the magnitudes. A point is inside the triangle if the quantities a, b, c, and d all have the same sign. If either b, c, or d is zero, the point lies on a side of the triangle and is also considered inside.

C. An Algorithm for a Bias and Temperature-Dependent Model

The inputs to the model are a table of bias-dependent temperature model coefficients stored in a model data file; the bias point VGS, VDS; and temperature T. Once the inputs are given, the TMC's of all the intrinsic ECP's and noise model parameters are interpolated at the desired bias point using (4). Equation (3) is then used to interpolate the values of each ECP

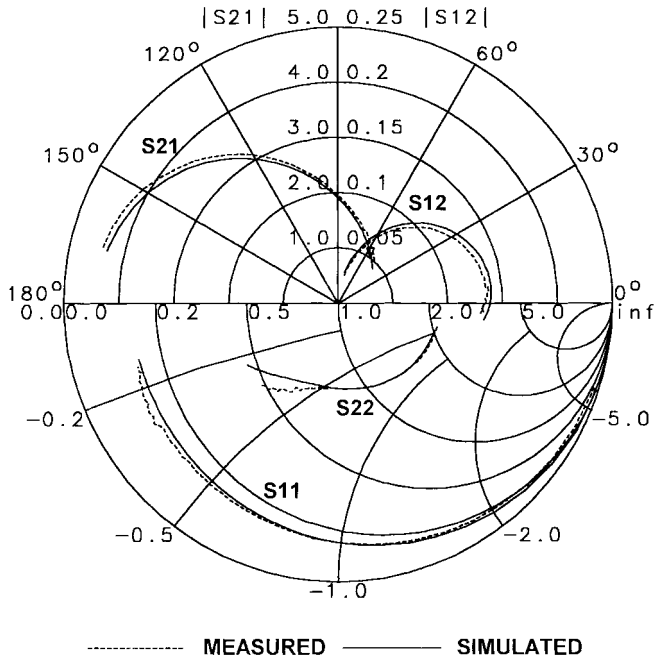

Fig. 4. Simulated (solid lines) versus measure S-parameter (dashed lines) data at a bias point ($\mathrm{VGS} = -0.4, \mathrm{VDS} = 1.2, T = 50\,^{\circ}\mathrm{C}$) not used in the modeling. The data presented is for the 0.25 μm × 300 μm MESFET.

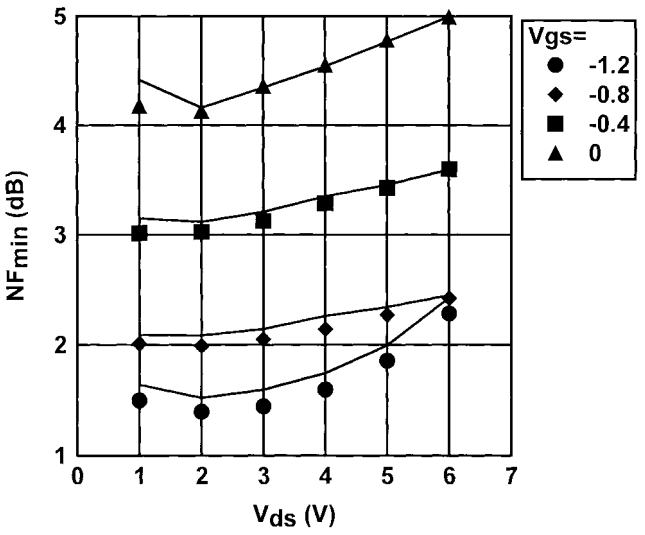

Fig. 5. Comparison of simulated (solid lines) and measured (symbols) minimum noise figure (NFmin) over bias. The data presented is for the 0.25 μm × 300 μm MESFET at $T = 80\,^{\circ}\mathrm{C}$ and $f = 12$ GHz.

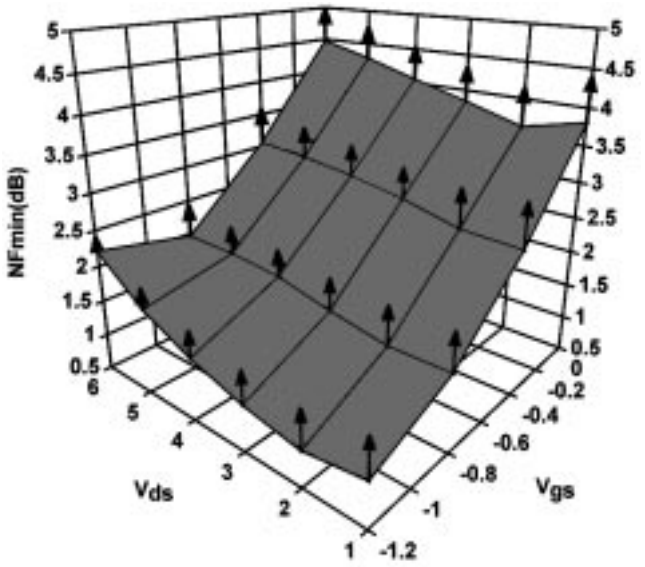

Fig. 6. Simulated minimum noise figure over bias and temperature. The shaded surface represent the simulated NFmin at $T = 25\,^{\circ}\mathrm{C}$ over bias. The arrows show the NFmin when T is changed from $25\,^{\circ}\mathrm{C}$ to $80\,^{\circ}\mathrm{C}$. The data presented is for the 0.25 μm × 300 μm MESFET at $f = 12$ GHz.

(including the extrinsic ECP's) and noise model parameters at the requested temperature. The model is now complete, and S-parameters and noise parameters simulations are possible via a microwave circuit simulator.

Currently our algorithm is restricted to bias points located inside or on the measurement bias grid. However, an extrapolation procedure can be added to handle bias points outside the measurement grid. Note that the algorithm does allow for extrapolation with respect to T through the use of (3).

D. Data Storage Requirement

The table-based model requires 22 parameters (14 TMC's for the intrinsic ECP's and 8 TMC's for the P, R, and Cs) to be stored at each bias point. For a 100-bias point grid (i.e., 10 VDS points and 10 VGS points), the quantity of stored numbers is 2216 (i.e., 2200 plus 16 TMC's for the extrinsic ECP's) as compared to the 836 000 stored numbers required by the example in the introduction. However, since the table-based model has the capability to interpolate, the number of bias points could be reduced to 5 VDS and 5 VGS points or a 25-bias point grid. This would reduce the amount of numbers stored to 566, an even greater saving in storage requirements. Since the data table is stored in one data file, it is easier to manage than the large number of data files required by the "brute force" method or the multitude of small-signal and noise models as required by the "conventional equivalent circuit model" approach.

III. Results

Two MESFET devices were modeled in this paper: a 0.25 μm × 300 μm MESFET, and a 0.5 μm × 300 μm MESFET [16]. S-parameters and noise parameters were measured over a grid of bias and over temperature. For the 0.25-μm device, the bias grid was VGS from 0 V to −1.2 V in 0.4-V increments and VDS from 1.0 V to 6.0 V in 1.0-V increments. For the 0.5-μm device a smaller bias grid was used: VGS from −0.4 V to −1.0 V in 0.2-V increments and VDS from 3.0 V to 5.0 V in 1.0-V increments. Both devices were characterized at three temperatures: 25 °C, 50 °C, and 80 °C for the 0.25-μm device; and 25 °C, 55 °C, and 85 °C for the 0.5-μm device. ECP's were extracted over bias and temperature and the above modeling procedure applied. The result of the modeling effort is a table of bias-dependent TMC's for each of the MESFET's.

The model was implemented within HP-EEsof's Libra 5.0™ as a user-defined element. For the 0.25-μm device, comparisons of simulated results to measured data are very

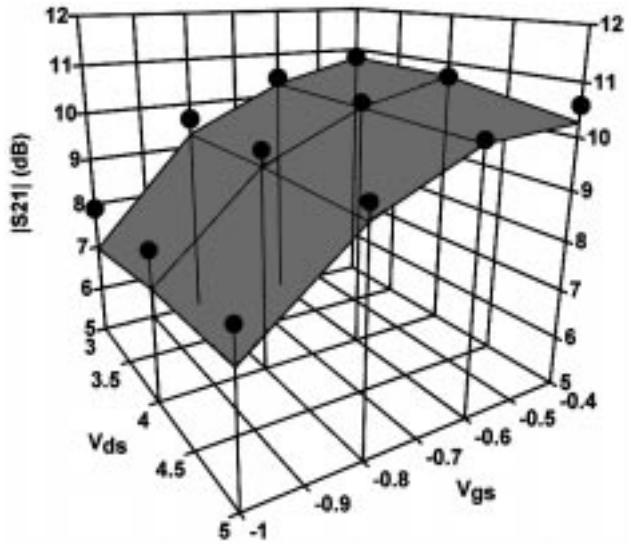

Fig. 7. Comparison of simulated (lines) and measured (symbols) single stage amplifier gain over bias. The results are for $f = 6$ GHz and $T = 25\,^{\circ}$C. A table-based model for the 0.5 μm $\times$ 300 μm device was used in the amplifier simulation.

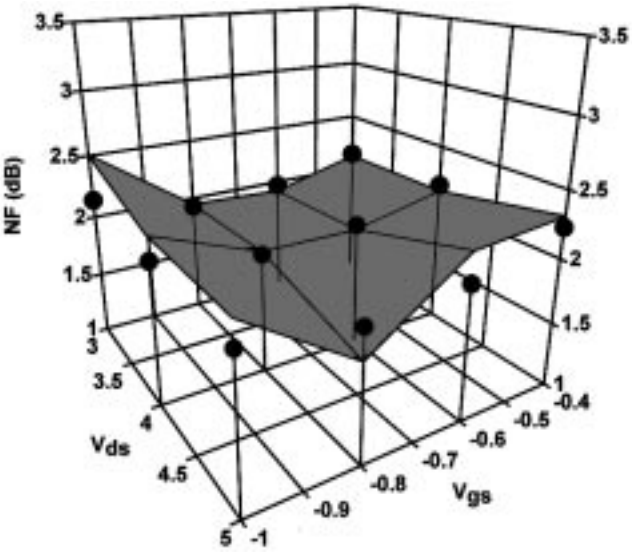

Fig. 8. Comparison of simulated (lines) and measured (symbols) amplifier 50-Ω noise figure. The results are for $f = 6$ GHz and $T = 25\,^{\circ}$C. A table-based model for the 0.5 μm $\times$ 300 μm device was used in the amplifier simulation.

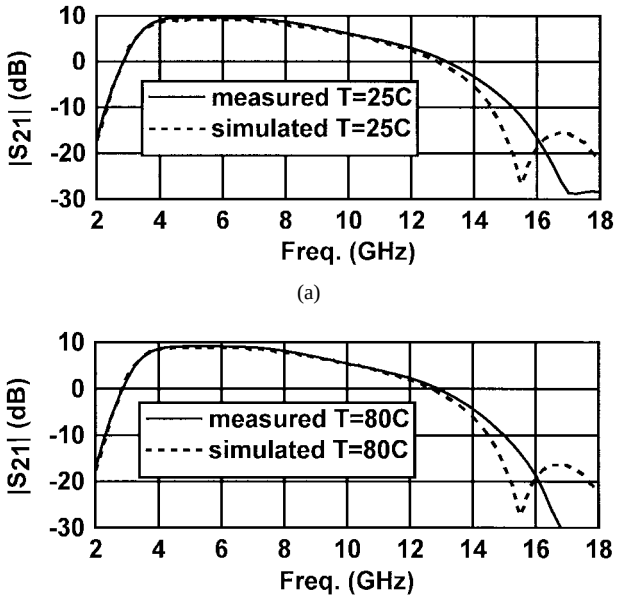

Fig. 9. Comparison of simulated and measured single-stage amplifier gain at two temperatures. The results are for the amplifier biased at $\mathrm{VGS} = -0.8$ and $\mathrm{VDS} = 4.0$. A table-based model for the 0.5 μm $\times$ 300 μm device was used in the amplifier simulation.

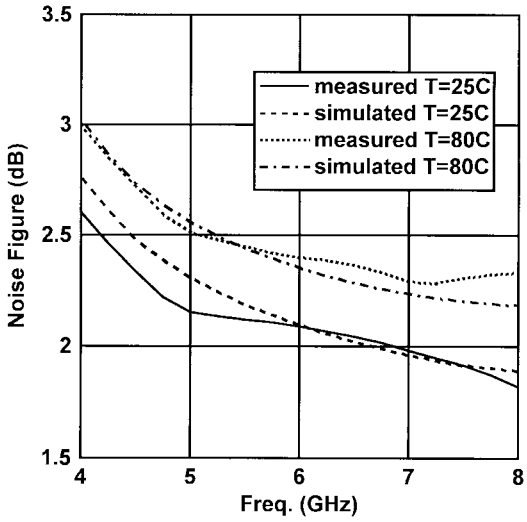

Fig. 10. Comparison of simulated and measured 50 noise figure for the single-stage amplifier at two temperatures. The results are for the amplifier biased at $\mathrm{VGS} = -0.8$ and $\mathrm{VDS} = 4.0$. A table-based model for the 0.5 μm $\times$ 300 μm device was used in the amplifier simulation.

good. To show the model's accuracy in reproducing the S-parameters versus bias, Fig. 3 shows a comparison between simulated maximum available gain or $G_{\max}$ and $G_{\max}$ calculated from measured S-parameters for $T = 25\,^{\circ}$C. Since $G_{\max}$ is calculated from all four S-parameters, the good fit indicated in Fig. 3 demonstrates the accuracy of the model over bias. Fig. 4 highlights the ability of the model to interpolate a point not used in the modeling. If further accuracy is required a smaller grid spacing could be used. Fig. 5 shows the minimum noise figure, NFMIN, as a function of bias at 12 GHz and $T = 80\,^{\circ}$C. As can be seen the model's fit to measured data is very good.

An advantage of this model over the other methods is the ability to easily simulate important device figures of merit over bias and temperature. As an example, Fig. 6 displays NFMIN versus bias and temperature. The arrows in Fig. 6 indicate the change in the NFMIN surface when T changes from 25 °C to 80 °C. From Fig. 6 it is easy to see that the minimum noise figure bias point is $\mathrm{VDS} = 2.0$ V and $\mathrm{VGS} = -1.2$ V.

To demonstrate the utility of our model in a circuit design situation, a table-based model of the 0.5-μm device was inserted into a single-stage MMIC low-noise amplifier design. Figs. 7 and 8 show comparisons of simulated versus measured amplifier gain and 50-Ω noise figure at $f = 6$ GHz and $T = 25\,^{\circ}$C over bias. The comparisons of simulated versus measured amplifier gain and 50-Ω noise figure are in general

good, with a maximum deviation of about 1 dB for gain and 0.3 dB for noise figure at $\mathrm{VGS} = -1.0$ V and $\mathrm{VDS} = 3.0$ V. Fig. 9 shows a broadband simulation of the amplifier gain compared to measured data for $T = 25\,^{\circ}\mathrm{C}$ and $80\,^{\circ}\mathrm{C}$ at a bias of $\mathrm{VGS} = -0.8$ V and 4.0 V. The comparison is very good over a broad range of frequencies from 2 to 12 GHz. The design band for this amplifier was 4–8 GHz. Fig. 10 compares the simulated 50 noise figure versus measured noise figure over the design band of the amplifier. Again the comparison is very good.

IV. Conclusion

A novel table-based small-signal and noise model has been described. The model includes bias and temperature dependence and is shown to be accurate at points not tabulated in a coarse grid of data points, such as that used in the demonstration data herein. The model is a very useful and efficient tool, both for studying the effects of temperature and bias variation on circuit performance, as well as designing temperature compensating bias networks for FET-based small-signal circuits.

Because one compact data table represents a single sample device, the approach can be adapted for use in a statistical FET model data base. Such a statistically derived table-based FET model would allow FET-to-FET variations in bias and temperature-dependent performance to be accurately represented as well as the variations in nominal (single bias, room temperature) performance.

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